REMARKS/ARGUMENTS

Amendments were made to the Specification to correct errors and to clarify the Specification. No new matter has been added by any of the amendments to the Specification.

Claims 1, 3-5 and 7-22 are pending in the present application. Claims 1, 5, 7, 9, 10 and 20 have been amended, and Claims 2 and 6 have been cancelled, herewith. Reconsideration of the pending claims is respectfully requested.

I. Objection to Specification

The Examiner objected to the Specification, stating that the use of Java should be capitalized and used with generic terminology in order to respect the proprietary nature of the trademark. In response thereto, Applicants have amended the Specification herewith.

Therefore, the objection to the Specification has been overcome.

II. 35 U.S.C. § 101

Claims 20-22 stand rejected under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

Applicants have amended Claim 20 in accordance with the PTO guidelines provided in the MPEP, and thus Claim 20 (and dependent Claims 21 and 22) is statutory[1].

Therefore, the rejection of Claims 20-22 under 35 U.S.C. § 101 has been overcome.

III. 35 U.S.C. § 103, Obviousness

Claims 1-8 and 10-22 stand rejected under 35 U.S.C. § 103 as being unpatentable over US Patent No. 5,590,335 of Dubourreau et al. in view of Applicant's Admitted Prior Art. This rejection is respectfully traversed.

Applicants initially show that the information contained in the background section of the present application is not admitted prior art, and even if it were, it is excluded under 35 USC 103(c) as it is part of the present application and thus is commonly owned by Applicants. The present application and the cited background section of this same present application were, at the time the invention was made, owned by or subject to an obligation of assignment to, the same person. Accordingly, Applicants background

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[1] **MPEP 2106(IV)(B)(1)(a):** A claimed computer-readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory.

section of the present application is excluded as a valid reference for a 35 USC 103 rejection, pursuant to 35 USC 103(c). Claims 1-8 and 10-22 have thus been erroneously rejected using such invalid reference.

Still further, Applicants have amended Claim 1 to include the features previously recited in Claim 2 (which is thus being cancelled herewith without prejudice or disclaimer). In rejecting Claim 2 (whose features are now a part of amended Claim 1), the Examiner states that the features of Claim 2 are taught by the cited Dubourreau reference at column 6, lines 63-67. Applicants urge that there, Dubourreau states:

> "When deadlocks occur, said machine can become almost unavailable; in that case, one can resort to a tool, either interactively, which is then a development tool used to implement the process, or retrospectively by calling on a tool for analyzing memory dumps and in this case, an image is taken of the machine's memory whose status is analyzed by a tool for analyzing memory dumps, either on another machine or on the same machine which has been restarted."

As can be seen, while this passage very briefly alludes to an interactive capability, all that is said for such interaction is an ability to 'implement the process'. This passage also states that the tool can be used retrospectively 'for analyzing memory dumps'. Such sweeping, broad-brushed statements do not teach or otherwise suggest any specific features pertaining to a user interface that allows a user to specify criteria such that the tool excludes threads that do not meet such user-specified criteria from identification as being deadlocked threads. Quite simply, the cited reference does not teach or otherwise suggest *user-specified criteria* that are used to *exclude threads from being identified as deadlocked threads.*

Still further with respect to Claim 1, such claim recites "wherein the tool identifies threads that are in a self wait condition and threads that are in a circular wait condition". As can be seen, the tool identifies *two different types of threads* – those that are in a self wait condition *and* those that are in a circular wait condition. The cited Dubourreau reference is being applied as teaching each of these two different types of wait conditions, and yet this cited reference in fact only teaches a single type of wait condition – a circular wait condition. This can be seen by Dubourreau's discussion at col. 1, lines 30-40 where a cycle is formed on the graph and the two threads T1 and T2 are irretrievably stopped such that there is a deadlock. The cycle formed on the graph is T1 -> L1 -> T2 -> L2 -> T1. In other words, Dubourreau's 'cycle' and the claimed circular wait are synonymous. However, all Dubourreau's discussion as to deadlock processing is with respect to this 'cycle' (col. 2, lines 11-22; col. 4, lines 24-33 and lines 44-45; col. 5, lines 6-10; col. 6, lines 44-45; col. 7, lines 47-49). Quite simply, Dubourreau teaches that 'cycles' are identified in determining a deadlock, and these 'cycles' are described as being of

the form of a graph such as T1 -> L1 -> T2 -> L2 -> T1, which is a circular wait condition. Dubourreau makes no mention of any type of self wait thread condition[2], and thus this cited reference does not teach or suggest the claimed feature of "wherein the tool identifies *threads that are in a self wait condition and threads that are in a circular wait condition*".

Nor would a person of ordinary skill in the art have been motivated to modify such teachings to include the above identified missing claimed features, as the teachings of this reference are concerned with overcoming problems with deadlock detection in a *multi-processor* environment where each processor can execute its own thread, by extending the cycle (i.e. circular wait) detection methodology to operate in such a multi-processor environment (Abstract; col. 1, lines 42-62; col. 4, line 66 – col. 5, line 10). There is no described concern or methodology directed to self-wait conditions, but rather to wait conditions *between multiple processors*. The fact that a prior art device could be modified so as to produce the claimed device is not a basis for an obviousness rejection unless the prior art suggested the desirability of such a modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Although a device may be capable of being modified to run the way [the patent applicant's] apparatus is claimed, there must be a suggestion or motivation *in the reference* to do so. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Thus, it is further urged that Claim 1 is not obvious in view of the cited references as there are additional claimed features not taught or suggested by the cited references, nor is there any motivation to modify the teachings of such references in accordance with the above identified missing claimed features.

Applicants traverse the rejection of Claims 3 and 4 for reasons given above with respect to Claim 1 (of which Claims 3 and 4 depend upon).

Applicants traverse the rejection of Claim 5 (and dependent Claims 6-10) for substantially the same reasons as those given above with respect to Claim 1.

With respect to Claim 11 (and dependent Claims 12-16), it is urged that the cited Dubourreau reference does not teach or suggest any type of thread in a self wait condition, as previously described with respect to Claim 1, and thus it is respectfully submitted that Claim 11 (and dependent Claims 12-16) is not obvious in view of the cited references.

Further with respect to Claim 16, Applicants further traverse the rejection of such claim for substantially the same reasons as those given above with respect to the user-interface discussion pertaining to Claim 1.

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[2] The Examiner states that this self wait condition is taught by the cited Dubourreau reference since if the cycle displays only one thread, a self wait condition is identified. Applicants respectfully urge error in such statement, since as described above every mention by Dubourreau of a 'cycle' is with respect to circular wait condition and thus the display of only one thread would never occur per such teachings.

Applicants traverse the rejection of Claims 17-22 for similar reasons to those given above with respect to Claim 11.

Therefore, the rejection of Claims 1-8 and 10-22 under 35 U.S.C. § 103 has been overcome.

IV. 35 U.S.C. § 103, Obviousness

Claim 9 stands rejected under 35 U.S.C. § 103 as being unpatentable over US Patent No. 5,590,335 of Dubourreau et al. in view of Applicant's Admitted Prior Art, and further in view of US Patent Application No. 2003/0023656 of Hutchison. This rejection is respectfully traversed.

Applicants initially traverse such rejection for similar reasons to those given above with respect to Claim 1 (of which Claim 9 depends upon), and urge that the newly cited Hutchison reference does not overcome the numerous teaching/suggestion deficiencies identified with respect to Claim 1.

Further with respect to Claim 9, it is urged that the newly citged Hutchison reference is direct to a technique to *avoid potential deadlock conditions* (Abstract), whereas the invention recited in Claim 9 is directed to a technique for *identifying actual deadlock conditions* (see, e.g., Claim 1 in combination with Claim 9, "wherein the matrix is used to identify threads in a circular wait condition"). As described by Applicants at Specification page 5, line 6, deadlock avoidance techniques may not be practical in certain systems such as those having large numbers of concurrently executing threads. It is therefore urged that a person of ordinary skill in the art would not have been motivated to combine such dissimilar techniques together, as they have different objectives and purposes, and therefore Claim 9 is not obvious in view of the cited references[3].

Still further, Claim 9 recites that the matrix includes two different things, in order to advantageously allow for identifying threads that are in a circular wait condition. Specifically, the matrix of Claim 9 is populated to include both (1) threads owning resources and (2) threads waiting on resources. In contrast, the matrix as described by Hutchison is a node-arc matrix that indicates a 'to' and 'from' relationship between threads. For example, a '1' in a row-column intersection indicates that there is a path ('waiting relationship') between the threads associated with the row-column intersection (page 5, paragraph 0067). This matrix does not provide any type information with respect to *threads that own resources* – and in fact there would be no reason for such matrix information, since these teachings are

[3] It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claims as a "blueprint". When prior art references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985). When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. "...absence of such suggestion to combine is dispositive in an obviousness determination". *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 42 USPQ2d 1378 (Fed. Cir. 1997).

directed to avoiding deadlocks in the first place. In contrast, and is depicted in Applicants preferred embodiment along the top of the matrix depicted in Figure 5 (and as described in the Specification at page 16, lines 18-26), threads that hold resources are identified by an entry in a respective column of the matrix (e.g. thread "inst:1 – thd:1" is identified as owning resource "java.lang.Object@4D7F018/4D7F020"). Again, the matrix as described in the cited Hutchison reference only indicates whether there is a path between two threads, such as the paths depicted by the arrows in Hutchison's Figure 5A. Thus, it is further respectfully submitted that Claim 9 is not obvious in view of the cited references as there are additional claimed features not taught or suggested by the cited references.

Therefore, the rejection of Claim 9 under 35 U.S.C. § 103 has been overcome.

V. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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